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EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 06/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,488	GREENFIELD ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) *38-41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on February 24, 2004 had been considered by the examiner.

Claim Objections

2. Claims 38-41 are objected to because of the following informalities:

Claim 38, cites "wherein said cache memory is arranged in blocks, by:" from the phrase it is understood that memory is arranged in blocks by steps of following lines.

Claim 39, line 3, "blocks of ways:" should be "block of ways;"

Claim 40, cites "wherein said main memory is arranged in blocks, by:" from the phrase it is understood that memory is arranged in blocks by steps of following lines.

Claim 41, line 3, "main memory block:" should be "main memory block;"

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 2-3, 7, 10, 13, 18-19, 24, 31, 32, 35, 37, and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Line 4, claims 2,10, it is not clear what applicant meant by the phrase "specified block of ways". Is the data block is associated with multiple ways or block from one of way of multiple ways of the cache?

Lines 5-6 of claims 3 and 19 cites, "when said data is not equivalent". It is not clear what applicant meant from the phrase "when said data is not equivalent". Data is not equivalent to what?

Claim 7, line 2, it is not clear from the phrase "cache memory comprises a dirty bit to indicate said equivalent status", equivalent status of what?

Claims 13 and 24 cite "said data is not found to be present", it is not clear where data not found to be present?

Claim 18 cites "a group of cache memories" it is not clear what applicant refer to as group of memories.

Claims 31, 35 and 39 cites "wherein each cache memory block comprises a block of ways" in lines 1-2. It unclear what applicant meant by "memory block comprises a block of ways"?

Claim 32 cites "and said comprises examining", it unclear what examining applicant refers to?

Claims 37, 41 cites "memory block comprises a block addresses" in line 2. Is memory block is the address or it is associated with some memory address?

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Claim 1 recites the limitation "said associative memory" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 3 recites the limitations "data cached in said way", "the corresponding main memory data", "said updating' and "said data" in lines 3-6. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 7 recites the limitation "said way" in line 3. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 9 recites the limitations "updated data" and "said way" in line 2. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 11 recites the limitations "said way", "a validity bit" and "said way" in lines 2-3. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 12 recites the limitation "main memory" in line 5. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 15 recites the limitation "said cache memories" in line 3. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 19 recites the limitations "said way", "the corresponding main memory data" and "said data" in lines 3-4 and 6. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 20 recites the limitation "said way" in line 3. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 21 recites the limitation "said updated data" in line 3. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 22 recites the limitations "updated data" and "said way" in line 2. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 23 recites the limitation "data" in line 4. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 24 recites the limitations "data", "said data caching" and "said data" in lines 3 and 5. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 25 recites the limitations "said cache memory preprocessor" and "a cache memory" in lines 1-2. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 26 recites the limitations "a segmented memory", "processing system", "a memory segment" and "said cache memory sections" in lines 2, 5-6, 8 and 9. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 27 recites the limitation "said cache memory sections" in line 1. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 28 recites the limitation "said multiple way cache memory processing command" in line 5. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 29 recites the limitation "said cache memory device" in line 2. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 30 recites the limitation "said command" in line 2. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 31 recites the limitations "said way", "main memory data" and "said main memory" in lines 4 and 7. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 33 recites the limitations "updated data" and "said way" in line 2. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 34 recites the limitations "said command" and "data in a specified block" in lines 2 and 3. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 35 recites the limitation "said specified block" in line 4. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 36 recites the limitations "said main memory" and "said command" in lines 1-2. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 37 recites the limitation "said specified block of main memory" in line 3. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim 38 recites the limitations "said main memory" and "said command" in line 5. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 39 recites the limitations "data cached", "said way", "main memory data", "said updated data" and "said main memory" in lines 4 and 6. These terms are open to interpretation. There is insufficient antecedent basis for these limitations in the claim.

Claim 40 recites the limitation "said command" in line 5. This term is open to interpretation. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 42-49 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. As the claims are directed to program instructions and compiler, which is descriptive material, and not embodied as a computer readable storage medium, it is considered descriptive material and therefore unpatentable. Claims 42-49 will not be treated further on the merits.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 17-25 and 38-41 are rejected under 35 U.S.C. 102(e) as being anticipated by So et al. (US 2004/0143711 A1) (So herein after).

As per claim 17, So teaches a background memory refresher, for updating main memory data in accordance with data cached in a cache memory (So teaches a read-ahead cache (RAC) with controller and controller performs the function of updating, invalidating and prefetching functions, fig.1 paragraphs [0003] and [0014], updating cache and main memory is taught in paragraph [0024]), wherein said cache memory is arranged in blocks (paragraph [0016]), comprising:

a command inputter, for receiving a block update command; and

a block updater, associated with said command inputter, for performing background operations block wise from a specified block of said cache memory so as to update said main memory in accordance with the data cached in said specified block of said cache memory (So teaches RAC with controller (fig.1, paragraph [0014]), which operates in background (paragraph [0003]) and receives commands from processor and performs invalidation on blocks of data (paragraph [0020]) and updates cache and

main memory according to data cached in RAC based on addresses (specified blocks) provided (paragraph [0024]), thus So inherently teaches a memory refresher, a command inputter and block updater).

As per claim 18, So teaches a read-ahead cache memory (paragraph [0013]) and according to present application specification cache memories can be any of three cache mapping strategies (see page 2, paragraph 2), thus So inherently teaches one of three mapped cache.

As per claim 19, So teaches cache controller, which identifies the data to be replaced (or updated) in RAC and main memory after selectively invalidating data blocks (paragraphs [0020] and [0024]), which inherently teaches a way checker (which cache block to be replaced) and a data storer (which block of cache line needs to be updated).

As per claims 20 and 22, cache memories are known to include validity bit to indicate valid or invalid data (see present application specification page 3, paragraph 1). So teaches invalidating cache line blocks as taught in claim 17, and updates those data blocks from main memory, which inherently teaches marking validity bit to indicate valid or invalid data and after updating dirty data from main memory resetting of flag.

As per claim 21, So teaches data with relevant addresses (paragraph [0024]).

As per claims 23 and 24, So teaches prefetching data from main memory (claim 23) into cache (paragraph [0003]) and loading data from main memory to cache upon cache miss (checking of data present and caching if data not present (claim 24))

(paragraph [0017]). So also teaches a cache controller performing as a command inputter, a cache checker and data cacher as explained with respect to claim 17.

As per claim 25, So teaches on-chip RAC on cache (paragraph [0021]).

Claims 38-41 are rejected under same rationales as applied to claims 17-25 above.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-13 and 28-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Wallin et al. (US 2004/0260883 A1) (Wallin herein after).

As per claim 1, Wallin teaches a cache memory preprocessor, for preparing a cache memory for use by a processor (fig. 2, item 202, paragraph [0032], cache controller performs functions of prefetching, invalidating and updating, similar to preprocessor of current application), said processor being arranged to access main memory via data caching in said associative memory (paragraph [0029], taught as a processor may access the data by caching the data, fig.2, item 204 is associative memory), said cache memory preprocessor (controller, fig. 2, item 202) comprising:

a command inputter, for receiving a multiple-way cache memory processing command from said processor (paragraph [0034], taught as controller receives a request); and

a command implementer associated with said command inputter, for performing background processing upon multiple ways of said cache memory in accordance with said multiple-way cache memory processing command (paragraph [0052], taught as cache controller is configured to convey a bundled transaction to request all available (or subset) of line within the same cache tag, since cache controller receives and implements command sent from a processor, inherently teaches a command inputter and implementer).

As per claim 2, Wallin teaches a block updater to update cache data from main memory (paragraphs [0035] and [0046]).

As per claim 3, Wallin teaches cache controller checking valid or invalid cache line present in the cache as well as upgrading cache lines if line is in invalid state (paragraphs [0038] and [0046]), inherently teaches a way checker and data storer.

As per claims 4-6, Wallin teaches n-way set associative cache (fig. 2, item 204), as well as any direct or associatively mapped cache (paragraph [0026]).

As per claims 7-11, Wallin teaches a validity bit to indicate equivalence status (paragraph [0033]), also Wallin teaches invalidating and updating data in cache (paragraph [0046]). (Also using validity bit to manage cache memory by setting validity bit and resetting back after cache line is updated from main memory is known in the art as admitted by applicant, see specification page 3).

As per claims 12-13, Wallin teaches prefetching multiple lines upon miss in cache according to address tag (paragraphs [0007]-[0012], [0046] and [0052]). Thus, Wallin inherently teaches block initializer (to prefetch lines of memory into cache), cache checker (checking hit/miss to load or to replace the data from main memory into cache).

Claims 28-37 are also rejected under same rationales as applied to claims 1-13 above.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 14-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Wallin et al. (US 2004/0260883 A1) (Wallin herein after) as applied to claim 1 above, further in view of Greenfield (US 2004/0221112, this is copending application of one of co-inventor of present application, subject matter used is from background of invention section from the copending application to include as applicant's admitted (or well known in the art) prior art) (AAPA herein after) and Joseph (5,875,451) and Van Dyke (6,853,382).

As per claims 14-15, Wallin teaches claimed invention, but fails to teach segmented memory with respective cache and interconnector. AAPA (incorporated as admitted or well known in the art) teaches segmented memory with interconnect

(paragraphs [0003] and [0006], figs. 1 and 2). It would have been obvious to one having ordinary skill in the art at the time of the invention to have segmented memory as taught by AAPA in system of Wallin to take advantage of parallel processing for improved system performance. The combination of Wallin and AAPA fails to teach respective cache section. Joseph discloses a hybrid main memory comprising both EDRAM and DRAM memory portions. Most of the EDRAM portion is being used as main memory and the remainder of EDRAM acts as a cache for DRAM portion of main memory, which allows retaining the performance of the cache in the memory (column 2, lines 9-17).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention to use the main memory as being taught by Joseph into system of Wallin and AAPA in order to use a part of a portion of the main memory as a cache for better performance.

As per claim 16, combination of Wallin, AAPA and Joseph disclose the claimed invention, but fails to teach prioritizer. Van Dyke teaches a controller for memory system having multiple partitions, wherein each partition has an arbiter, having an output that supplies requests to the partitions and a number of inputs, each of which connects to a client. Each arbiter prioritizes the servicing of requests at its inputs according to a priority policy (fig. 3 and 5A; column 2, lines 10-17).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention to use the controller as being taught by Van Dyke into combination of Wallin, AAPA and Joseph's system in order to improve efficiency of memory accesses.

Claims 26-27 encompass the same scope of the invention as those of claims 1 and 14-16. Therefore, claims 26-27 are rejected for the same rationales as applied to claims 1 and 14-16.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

6/6/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER